REMARKS/ARGUMENTS

Claims 11-27 are pending. Claims 11-19 and 21-26 were rejected under 35 U.S.C. § 102. Claims 18, 20 and 27 were rejected under 35 U.S.C. § 103. Claims 11, 18, and 23 are herein amended to more clearly set forth the claimed invention. Support for the claim amendments can be found through out the specification and the drawings. No new matter is believed added.

Claim Rejections – 35 USC § 102

Claims 11-14, 18, 23, 25, and 26 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,995,415 to Kuo *et al.* (hereafter "Kuo"). Claims 11-17, 19, and 21-26 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,614,685 to Wong (hereafter "Wong"). These rejections are respectfully traverses.

35 U.S.C. § 102(b) rejection of claims 11-14, 18, 23, 25 and 26 based on Kuo

Claims 11-18:

Claim 11 as amended distinguishes over Kuo at least by reciting:

> a plurality of memory arrays partitioned into first and second memory banks in correspondence with one of a plurality of mask options such that the length of a plurality of bit lines in each of the first and second memory banks remains fixed for all of the plurality of mask options ...

Kuo is directed to "a simultaneous operation flash memory device with a flexible bank partition architecture" (col. 1, lines 6-7). As shown in FIG. 2, Kuo implements the "flexible bank partition architecture" using "flexibly partitioned bit lines such as bit lines 28 and 30" (col. 5, lines 28-30) (emphasis is added). This technique is more clearly described by Kuo in reference to FIG. 2 in column 5, lines 31-35:

> The gaps 28*c* and 30*c* as well as gaps in the other bit lines in the memory array 20 serve as a memory partition boundary between the lower and upper memory banks.

Thus, Kuo obtains the desired partitioning by varying the length of bitlines 28 and 30 (FIG. 2). Kuo varies the length of the bitlines using one of a variety of metal mask options as shown in FIGS. 6-10 and described in column 1, line 14 through column 12, line 8.

In contrast to Kuo's technique wherein the length of the bitlines in the upper and lower memory banks varies depending on the selected mask option, in Applicant's technique the length of the bitlines "in each of the first and second memory banks remains fixed for all of the plurality of mask options" as recited in Applicant's claim 11 (emphasis added).

Therefore, claim 11 and its dependent claims 12-18 distinguish over Kuo at least for the above reason.

Claims 23-26:

Claim 23 as amended includes similar limitations to those of claim 11 cited above, and thus claim 23 and its dependent claims 24-26 distinguish over Kuo at least for the same reasons stated above.

35 U.S.C. § 102(e) rejection of claims 11-17, 19, and 21-26 based on Wong

Claims 11-18:

Claim 11 distinguishes over Wong at least by reciting:

> a plurality of memory arrays partitioned into first and second memory banks in correspondence with one of a plurality of mask options ...

The Examiner in paragraph 5 of the Office action indicates that the above limitations of claim 11 are taught by Wong in "col. 1, line 59 to col. 2, line 6, col. 2, lines 32-35, col. 4, line 58-61 and col. 5, line 55-65". This is respectfully traversed because neither in these passages of Wong cited by the Examiner nor anywhere else in Wong is there a teaching or suggestion of the use of "mask options" for any purpose. This is because Wong uses circuit techniques, not mask options, to achieve "greater flexibility" in "allocation of blocks for storage of data, code, or parameter" (col. 4, lines 60-61).

Wong achieves "maximum flexibility by allowing use of each array plane for any type of data" (column 5, lines 48-49). That is, contrary to the prior art cited in Wong wherein each of two asymmetrical memory banks is dedicated to storing a particular type of data, Wong allows any one of the array planes to be used for storing any of data, code, and parameters. Wong achieves this by using a circuit technique (not mask option) whereby the read and write paths for each array plane 210 (Fig. 3) are separated so that the "read path can read from one array plane while the write path writes in another array plane" (Abstract). This circuit technique is shown in Fig. 3 and described in detail in column 6, line 21 through column 7, line 60. In Fig. 3, "[p]artition control circuit 320 [sic 330] determines whether the array plane will perform a read, a write, and an erase, or no operation (e.g., idle or standby)." Thus, Wong achieves the desired partitioning using circuitry (including the partition control circuit 330), not "mask options" as recited in Applicant's claim 11.

Thus, Claim 11 and its dependent claims 12-18 distinguish over Wong for at least the above reason.

Claims 19-21:

Claim 19 distinguishes over Wong at least by reciting:

> wherein one of a plurality of metal mask options is selected to configure the row and column selection circuits to obtain a desired partitioning of the plurality of memory arrays into first and second memory banks ...

Underlines are added. As discussed above, Wong uses circuit techniques to achieve the desired partitioning, and as such fails to teach or suggest use of mask options "to obtain a desired partitioning" as recited in Applicant's claim 19. Thus, claim 19 and its dependent claims 20-21 distinguish over Wong for at least this reason.

Claim 22:

Claim 22 distinguishes over Wong at least by reciting:

> the plurality of memory arrays are partitioned into first and second memory banks by configuring the row and column

> selection circuits into one of a plurality of mask-selectable configurations ...

Underline is added. As discussed above, Wong uses circuit techniques to achieve the desired partitioning, and as such fails to teach or suggest partitioning memory arrays by configuring particular circuits into one of a number of "mask-selectable configurations" as recited in Applicant's claim 22. Thus, claim 22 distinguishes over Wong for at least this reason.

Claims 23-26:

Claim 23 distinguishes over Wong at least by reciting:

> partitioning the plurality of memory arrays into first and second memory banks by selecting one of a plurality of mask options ...

As discussed above, Wong uses circuit techniques to achieve the desired partitioning, and as such fails to teach or suggest partitioning memory arrays "by selecting one of a plurality of mask options" as recited in Applicant's claim 23. Thus, claim 23 and its dependent claims 24-26 distinguish over Wong for at least this reason.

Claim Rejections – 35 USC § 103

Claims 18, 20, and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong. This rejection is respectfully traversed.

Claims 18 and 20 depend from claims 11 and 19, respectively. Thus, claims 18 and 20 distinguish over Wong for at least the same reasons as the respective claims 11 and 19 set forth above.

Claim 27 distinguishes over Wong at least by reciting:

> applying one of a plurality of metal masks ... wherein each of the plurality of metal masks corresponds to a different configuration of the row and column selection circuits ...

In paragraph 7 of the Office action, the Examiner does not address these limitations of claim 27. In fact, Wong nowhere teaches or suggests use of a number of metal masks wherein each of the metal masks corresponds to a different configuration of the row and

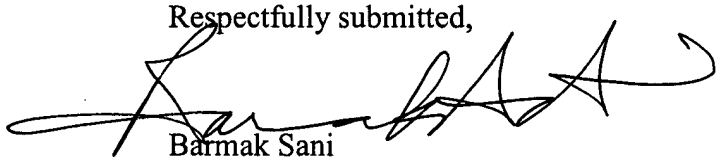
column selection circuits. The row and column selection circuits are respectively shown in Fig. 3 of Wong as X DECODE block 220 and Y DECODE block 240 in each array plane 220. Wong nowhere teaches or even suggests that the X DECODE blocks 220 and Y DECODE blocks 240 can have more than one configuration. Claim 27 thus distinguishes over Wong at least for this reason.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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